IN THE CLAIMS

Please amend the claims as follows:

Claims 1-2 (Canceled).

Claim 3 (Currently Amended): [[The]] A testing method ~~as in claim 2, wherein~~ for a semiconductor device, having wirings composed of copper or an alloy mainly composed of copper, comprising:

executing an acceleration test for eliminating an initial failure of the wirings due to stress migration, wherein executing the acceleration test comprises holding a temperature of the semiconductor device in a first temperature zone covering ±40°C of a temperature at which the stress migration is most accelerated, the temperature at which the stress migration is most accelerated is a test temperature when an acceleration factor AF is maximized, the acceleration factor AF is obtained based on a time to failure at a maximum temperature in actual use of the semiconductor device and a time to failure at the test temperature of the semiconductor device; and

checking whether or not the wirings are broken.

4. (Original) The testing method of a semiconductor device as in claim 3, wherein the acceleration factor AF has a relationship shown by following Expression

$$AF = \{C(TO - Ta)^{-n} \cdot \exp(Ea/kTa)\}/\{C(TO - Tatest)^{-n} \cdot \exp(Ea/kTatest)\}$$

where, Ta is the maximum temperature, Tatest is the test temperature, C and n are constants inherent to the semiconductor device, TO is a stress free temperature, Ea is activation energy of growth of voids in the wirings, and k is the Boltzmann constant.

5. (Currently Amended) The testing method as in claim [[2]] 3, wherein executing the acceleration test comprises holding the temperature of the semiconductor device in the first temperature zone for at least 0.4 hour.

6. (Currently Amended) The testing method as in claim [[2]] 3, wherein executing the acceleration test comprises holding the temperature of the semiconductor device in the first temperature zone from 0.4 hour to two hours.

7. (Currently Amended) The testing method as in claim [[2]] 3, wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device at least once in a second temperature zone covering ±40°C of a reference temperature set in the first temperature zone covering ±40°C of a temperature at which the stress migration is most accelerated.

8. (Original) The testing method as in claim 7, wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device in the second temperature zone for at least 0.4 hour.

9. (Original) The testing method as in claim 7, wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device in the second temperature zone from 0.4 hour to two hours.

10. (Currently Amended) The testing method as in claim [[1]] 3, wherein after semiconductor elements composing the semiconductor device are formed on a semiconductor

substrate, executing the acceleration test when the wirings are formed in wiring layers through interlayer insulation films and the semiconductor elements are connected to each other via the wirings.

Claims 11-20 (Canceled).